REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1, 3-9, and 11-17 are pending in the present application.

In the outstanding Office Action, Claims 1, 3-9, and 11-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fukuda et al. (U.S. Patent No. 6,099,574, herein Fukuda) in view of Hirotaka (Japanese Patent Application No. 08-282456, herein Hirotaka).

Applicants respectfully traverse the outstanding ground of rejection because the outstanding Office Action fails to provide a *prima facie* case of obviousness by asserting prior art that, no matter how the prior art references are combined, does not teach every element of independent Claim 1.

To establish a *prima facie* case of obviousness, M.P.E.P. §2143 requires that three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the references teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim elements. As explained below, the cited references do not teach or suggest all the claim elements.

With respect to the rejection of Claim 1 as unpatentable over Fukuda and Hirotaka, Applicants respectfully traverse the rejection because neither of these references discloses or suggests the claimed "generating virtual images outside the calculation area according to the boundary conditions; and displaying the virtual images, as well as real images included in the calculation area."

The technique disclosed by Fukuda includes a first simulator (process simulator) that simulates a semiconductor device to obtain the structure of the semiconductor device and the

impurity profile, etc. thereof.[1] A second simulator (device simulator) simulates the electrical characteristic etc. of semiconductor devices based on the results of the process simulator.[2]

The second simulator simulates for a finite calculation area of the semiconductor device. Calculations for the simulation need a large memory capacity and a long computation elapse time. To reduce the need for a large memory capacity and a long computation elapse time a finite calculation area is surrounded by a boundary. The boundary is usually defined by its behavior. The boundary conditions are represented with, for example, values and expressions. The boundary conditions include fixed boundary conditions, mirror boundary conditions, periodic boundary conditions, transmission boundary conditions, and infinite boundary conditions.

Fig. 3A of the present application explains boundary conditions. As shown in Fig. 3A of the present application, a wire-to-wire capacitance value may be correctly calculated if the distance D between the boundary and the wire A is sufficiently long. If the distance D is short, mirror images (if a mirror boundary condition is defined) form on the outside of the calculation area 130 due to the mirror boundary conditions. These mirror images affect the calculations (i.e., hinder correctly computing the capacitance value) regarding the wires inside calculation area 130. The computation of the capacitance value is hindered because, when a small potential dV is applied to wire B, wire A is affected by wire B, including the real image and all the virtual images. This problem is frequently overlooked by users, especially users unfamiliar with simulations.

The boundary conditions influence a simulation result. This influence by the boundary conditions is often overlooked by a design engineer. The design engineer is frequently unaware of a deviation in a simulation result from a true result to be derived from the simulation.

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[1] Fukuda, col. 6, lines 24-26, and col. 13, lines 41-57.
[2] Fukuda, col. 6, lines 34-37, and col. 14, lines 45-55.

The claimed invention enables users to examine the influence of boundary conditions on a simulation. According to the results of the examination, the claimed invention allows for correction of the simulation data in order to execute the simulation. In a non-limiting embodiment of the claimed invention, a display shows the virtual images that appear outside of the calculation area 130 due to the boundary conditions, as shown in Fig. 3B. The calculation area 130 of Fig. 3B corresponds to that of Fig. 3A. The calculation area 130 includes the real images of wires A and B. The non-calculation area outside the calculation area 130 includes virtual images that are formed according to the mirror boundary conditions. The mirror boundary conditions form a virtual wire A on the left side of the calculation area 130. On the left side of virtual wire A, a virtual wire B is formed due to real wire B. With images displayed as shown in Fig. 3B, the user can easily understand whether or not the capacitance value to be calculated corresponds to the intended calculation. As mentioned in the specification at page 6, line 24 to page 7, line 2, the term "virtual image" refers to an image that is outside the boundary 130 of Fig. 3B, and the term "real image" refers to an image that is inside the boundary 130 of Fig. 3B.

Applicants respectfully submit that Fukuda and Hirotaka, taken alone or in proper combination, do not disclose or suggest displaying images so a user can recognize an influence of the boundary defined by the boundary condition. The claimed invention generates virtual images outside the calculation area according to the boundary conditions, and displays the virtual images, as well as the real images, included in the calculation area. This allows a user to understand the influence of the boundary defined by the boundary conditions.

The outstanding Office takes the position that Fukuda discloses displaying the influence of the boundary condition at col. 14, lines 51-55.[3] However, this section of Fukuda

[3] Office Action, page 4.

discloses that "second simulator 60 displays ***on an output equipment thus obtained device behaviors, which may include potential profiles, electric field profiles, and current (carriers such as electrons and holes) profiles as well as current vs. voltage characteristics"*** (emphasis added). Fukuda only discloses that the second simulator displays device behaviors such as potential profiles. The second simulator does not describe or suggest displaying virtual images outside the calculation area according to the boundary conditions.

The outstanding Office Action also takes the position that Hirotaka discloses generating virtual images outside the calculation area according to the boundary condition at paragraph [0006] of Hirotaka, and displaying the virtual image, as well as real images included in the calculation area at paragraph [0006] and Figs. 2 and 3 of Hirotaka.[4]

Paragraph [0006] of Hirotaka merely describes setting boundary conditions. The boundary condition at the base of a substrate is a reflection-type boundary condition. If a count field is narrowed from the graph shown in Fig. 3, the solving accuracy becomes extremely poor, as seen from the result shown by the alternating long and short dash line C.

Paragraph [0019] and Fig. 2 of Hirotaka further describe that line C indicates a poor result because the boron concentration becomes overestimated.

Thus, Hirotaka does not disclose or suggest the claimed "generating virtual images outside of the calculation area according to the boundary conditions" and "displaying the virtual images, as well as real images included in the calculation area."

Furthermore, the outstanding Office Action takes the position that Applicants previously submitted argument that the claimed invention allows a user to recognize the boundary condition before the simulation is not permissible because Applicants have not

[4] Office Action, page 4.

specifically included recognizing the boundary condition before the simulation in the language of the claims.[5] Applicants respectfully traverse this position.

Claim 1 recites "if an instruction to make no change in the boundary conditions is entered, ***carrying out the simulation with the simulation data***" (emphasis added). This language indicates that the claimed invention makes a user recognize the boundary condition before the simulation.

In view of the above-noted distinctions, Applicants respectfully submit that Claim 1 (and Claims 3-8) patentably distinguish over Fukuda and Hirotaka, taken alone or in proper combination. Applicants respectfully submit that Claims 9 and 17 are similar to Claim 1. Thus, Claims 9 and 17 (and Claims 11-16) patentably distinguish over Fukuda and Hirotaka, taken alone or in proper combination, for at least the reasons stated for Claim 1.

Moreover, Applicants respectfully traverse position taken in the outstanding Office Action that Kenichi discloses "expanding the calculation area" from Claim 5. Applicants note that Claim 5 recites, *inter alia*, "expanding the calculation area and providing data concerning the expanded calculation area."

In a non-limiting embodiment shown in Fig. 7 of the present application, the original calculation area is displayed and the expanded area is also displayed. In the non-limiting embodiment, the simulation system generates the expanded area, based on the computation area, to correctly display the new calculation area for the user.

The outstanding Office Action takes the position that "when the selected area is smaller than the whole, repeating procedure to select the next analysis area for the area with the error over the constant value again, an solving the whole" of Kenichi is to be interpreted as the claimed "expanding the calculation area."[6] Applicants respectfully traverse this position. Kenichi only discloses that an area is selected for calculation, and then if an error is

[5] Office Action, page 3.
[6] Office Action, page 3.

bigger that a predetermined value, the next analysis area is selected with the error equal to the constant value again.[7] Kenichi does not disclose the claimed "expanding the calculation area and providing data concerning the expanded calculation area."

Furthermore, Applicants respectfully traverse the use of Kenichi in the outstanding grounds of rejection. The outstanding Office Action provides no motivation as to why a person of ordinary skill in the art would combine Kenichi with any of the other cited refereces.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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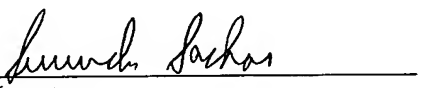

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[7] See, for example, Kenichi, paragraph [0012].